

1 14. The method of claim 13 wherein said data processing further includes a Target Delay
2 Interval (TDI) register containing a TDI value for determining when the vector mechanism should
3 not be polled by said dispatcher and an interrupt given to said processor, said method further
4 comprising overriding said TDI value and driving an immediate interrupt to said processor when
5 said override bit is in its first condition.

1 15. The method of claim 13 wherein said main storage is divided into multiple partitions, with
2 each partition having a vector mechanism operable to register I/O requests by said devices to send
3 or receive data from that partition of main storage, each partition having an associated override bit
4 for that partition, and said processor is a hypervisor, said method further comprising setting by said
5 hypervisor the override bit for that partition when said hypervisor is to handle an immediate
6 interrupt rather than polling by said dispatcher for that partition.

1 16. The method of claim 15 wherein said data processing system further includes one or more
2 central processing units (CPUs) assignable by said hypervisor to one or more of said partitions,
3 said method further comprising setting by said hypervisor, the override bit of one partition when
4 that partition does not have a CPU assigned to it.

1 17. The method of claim 13 further comprising resetting said override bit to its second
2 condition after an interrupt is handled by said processor.

1 18. The method of claim 17 further comprising resetting said override bit to its second
2 condition upon the first to occur for said interrupt handling or said dispatcher polling.

1 19. A program product for controlling the transfer of data in a data processing system having
2 a processor handling an I/O request in an I/O operation, main storage controlled by the processor
3 for storing data, and one or more I/O devices for sending data to or receiving data from said main
4 storage, said program product comprising:

5 a computer readable medium having recorded thereon computer readable program code
6 means for performing the method comprising:

7 registering in a vector mechanism, I/O requests by said devices to send or receive data
8 from said main storage;
9 polling with a dispatcher, said vector mechanism to determine if there is an outstanding I/O
10 request; and
11 sending an immediate interrupt to said processor when an override bit has a first condition
12 for handling an I/O request from said I/O device(s), or polling with said dispatcher, said vector
13 mechanism to determine if there is an outstanding I/O request when said override bit is in a second
14 condition..

1 20. The program product of claim 19 wherein said data processing further includes a Target
2 Delay Interval (TDI) register containing a TDI value for determining when the vector mechanism
3 should not be polled by said dispatcher and an interrupt given to said processor, said method
4 further comprising overriding said TDI value and driving an immediate interrupt to said processor
5 when said override bit is in its first condition.

1 21. The program product of claim 19 wherein said main storage is divided into multiple
2 partitions, with each partition having a vector mechanism operable to register I/O requests by said
3 devices to send or receive data from that partition of main storage, each partition having an
4 associated override bit for that partition, and said processor is a hypervisor, said method further
5 comprising setting by said hypervisor the override bit for that partition when said hypervisor is to
6 handle an immediate interrupt rather than polling by said dispatcher for that partition.

1 22. The program product of claim 21 wherein said data processing system further includes one
2 or more central processing units (CPUs) assignable by said hypervisor to one or more of said
3 partitions, said method further comprising setting by said hypervisor, the override bit of one
4 partition when that partition does not have a CPU assigned to it.

1 23. The program product of claim 19 wherein said method further comprises resetting said
2 override bit to its second condition after an interrupt is handled by said processor.

- 1 24. The program product of claim 23 wherein said method further comprises resetting said
2 override bit to its second condition upon the first to occur of said interrupt handling or said
3 dispatcher polling.